IDEC Chip Design Contest

A Low Power Voltage Step-up System for NAND Flash

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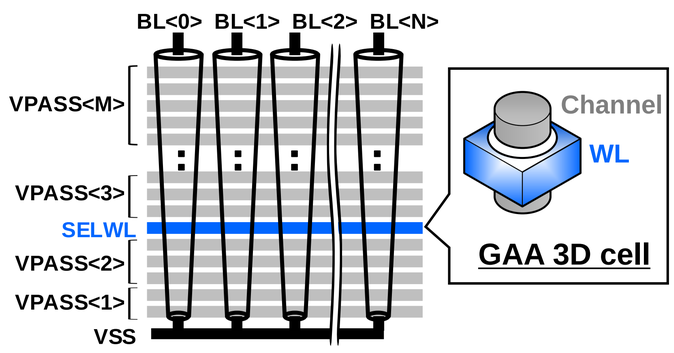
Abstract

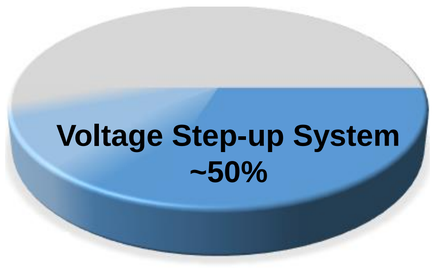
In order to reduce the energy of the voltage step-up system that uses up to 50% of the operating energy in 3D NAND flash,'Variable stage charge pump system' and 'Charge compensating regulator' without voltage ripple during steady state were proposed.
The chip fabrication for verification uses the Globalfoundaries 180nm UHV process, and a 56WL NAND flash system modeled with 10.1㎊/WL (WL to GND), 3.0㎊/WL (WL to adjacent WL), and 131㏀/WL is constructed to create a traditional energy compared to the system was confirmed to improve by 28%.

Introduction

The cell density of NAND flash is improved by applying a Gate-All-Around 3D cell.

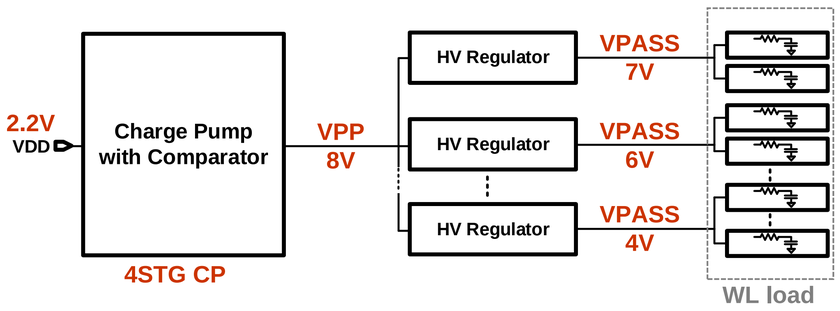
3D cell block with N-bit BL



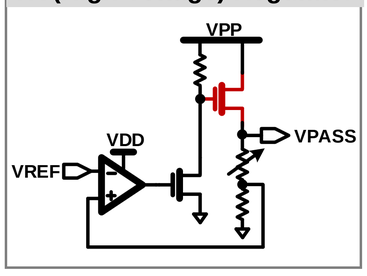


The energy consumption of the voltage step-up system for 'Word Lines' is up to 50%.

Conventional voltage step-up system



HV(High Voltage) Regulator

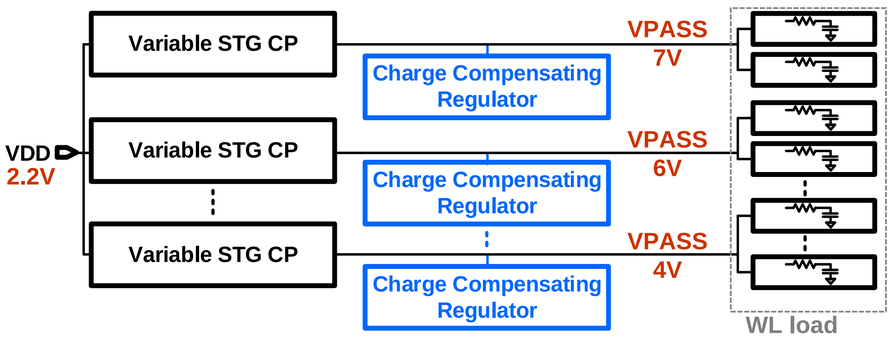


The regulator output uses NMOS. VPP must be sufficiently higher than the VPASS voltage.

How to reduce energy(or power) consumption?

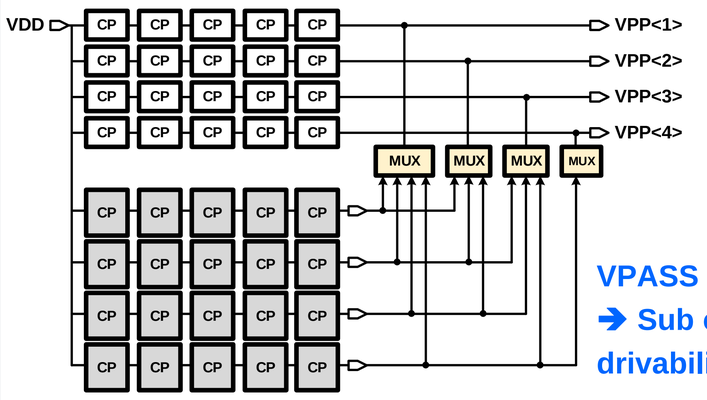
Proposed architecture & Implementation

Proposed voltage step-up system



- **VPASS is generated by charge pump ➔ 1 or more stage reduction**
- **CCR circuit suppressed voltage ripple.**

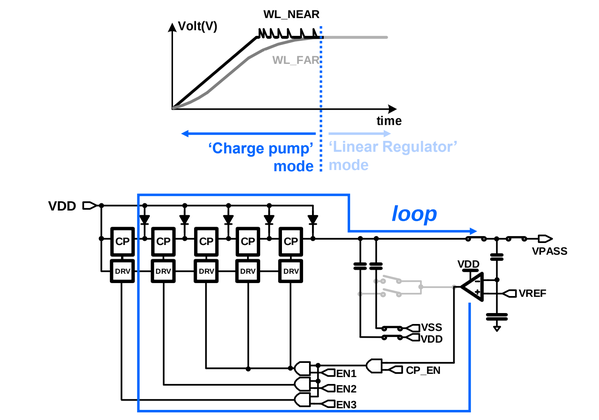
Charge pump with variable stage and variable current drivability



VPASS is generated by charge pump ➔ Sub charge pump reinforces the current drivability

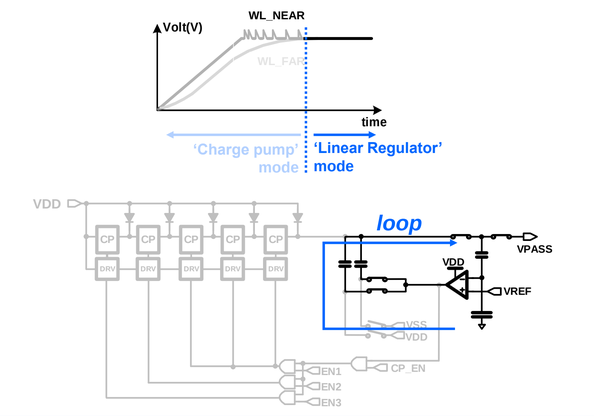
Operation of 'Charge Compensating Regulator'

'Charge pump' mode



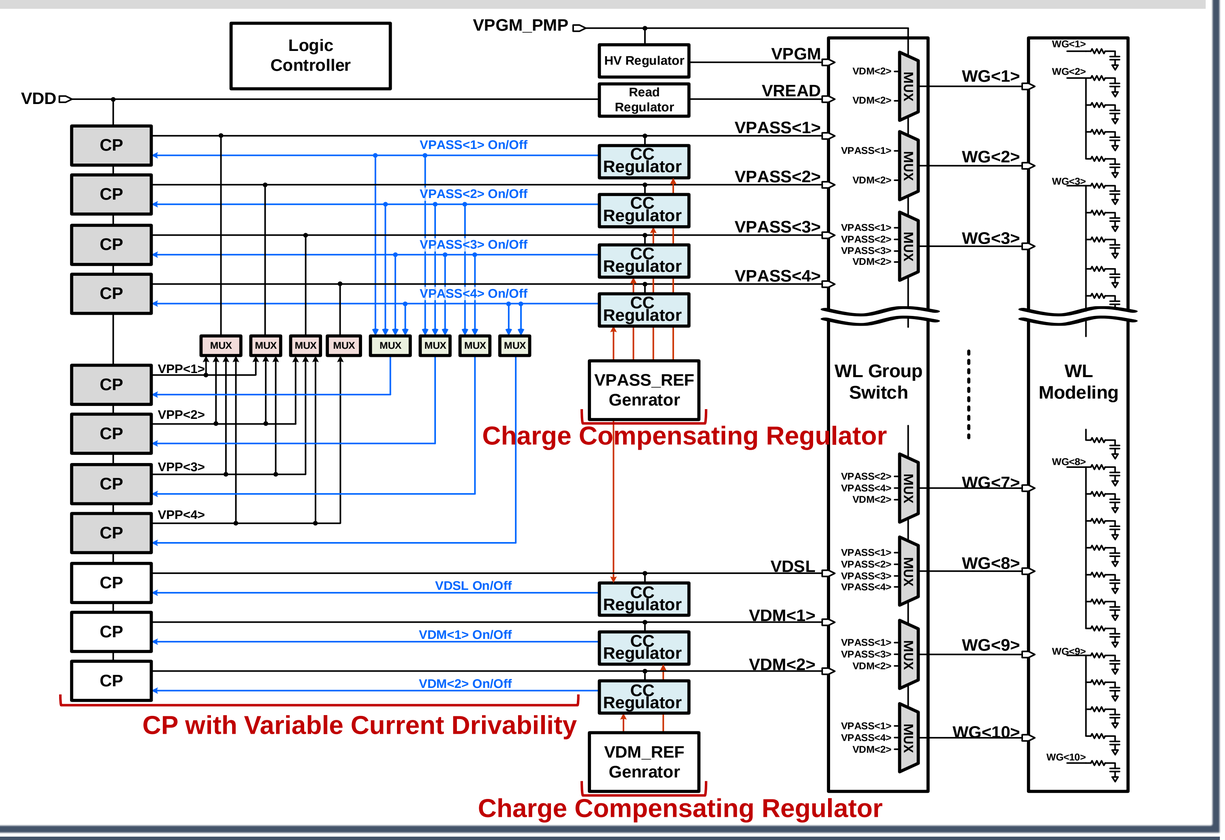
✓ During the transient
- **The voltages of WL Near and Far are different**
- **Voltage ripple is allowed**

'Linear regulator' mode



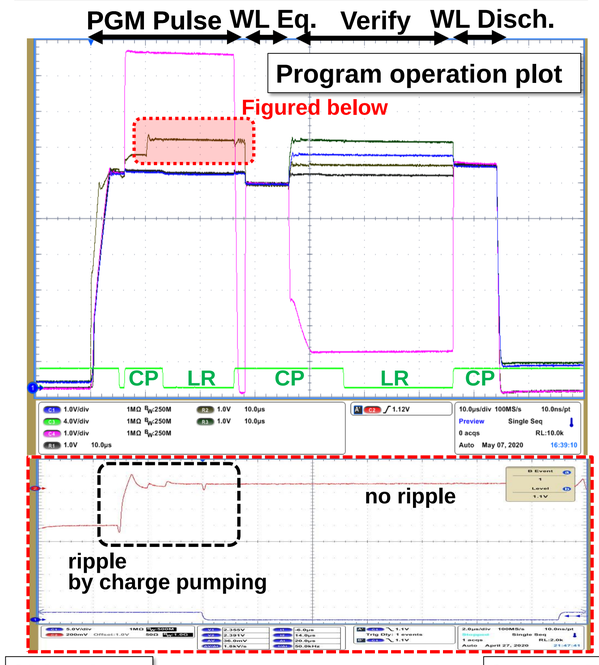
✓ During the steady state
- **The voltages of WL Near and Far are almost the same**
  ➔ When a voltage ripple occurs in WL Near, a program or read operation error occurs

Overall architecture



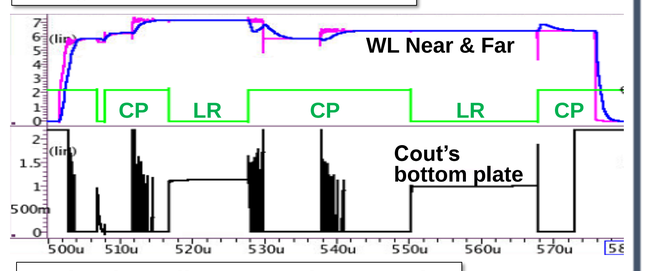
Results

Measurement results (WL Near)

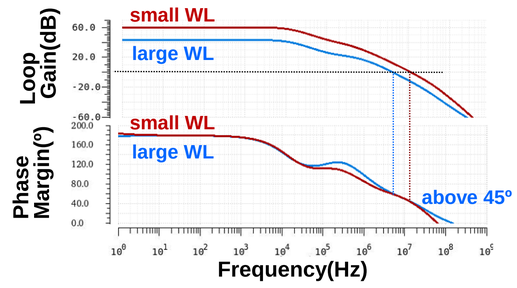


Simulation results

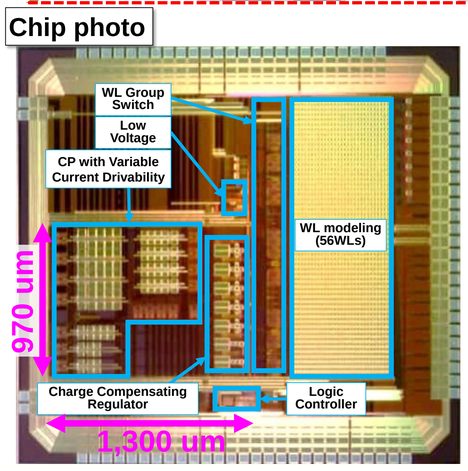
Voltage level of Cout's bottom plate



Bode plot @linear regulator mode



Chip photo



Comparison Table

	Proposed *(nJ)*	Conventional *(nJ)*	Energy reduction
Charge Pump for WL	45.76	52.45	-13%
HV Regulator (or CCR)	49.28	85.01	-42%
Reference Generator	3.70	3.70	
Other circuits	3.52	0	
Total	102.26	141.15	-28%

Assumption
Quiescent current @HV Regulator : 5 uA/branch

Acknowledgement

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.